wherein each of the substantially parallel stacked layers comprises one or more processors and/or one or more memories, and electrical conducting structures which form internal electrical connections in the layer,

wherein each substantially parallel stacked layer is formed of a plurality of sublayers, having delimited portions which form dielectric, semiconducting or electrical conducting areas in the sublayer and the sublayer, in addition to at least one dielectric portion, having one or more semiconducting and/or electrical conducting portions,

Cont. a1

wherein delimited portions with a given electrical property in each sublayer are provided in a registering relationship to one or more corresponding portions in at least one of the adjacent neighbour sublayers to form integrated circuit elements which extend vertically through one or more sublayers,

wherein the electrical conducting structures are formed by the electrical conducting portions in the sublayer and respectively extend horizontally in order to create horizontal electrical conducting structures or are provided in registering connection with corresponding electrical conducting portions in one or more adjacent sublayers, such that the electrical conducting structures integrated in the sublayers form three-dimensional electrical interconnecting networks in the layers and interconnect the circuit elements therein mutually in three dimensions, and

wherein additional electrical conducting structures in the data-processing device interconnect the layers mutually and/or the layers with the substrate and in order to create a connection to the exterior of the data processing device.

cont. A1

18. A scaleable integrated data processing device according to claim 17, wherein the sublayers in one or more of the substantially parallel stacked layers are realized in a technology which on a first level of a functional hierarchy configures functionally one or more of the layers as a combined processor and memory layer (MP), or one or more the layers substantially as processor layers (P) or one or more the layers substantially as memory layers (M).

19. A scaleable integrated data processing device according to claim 18, wherein the processing unit in a layer (P, MP) is configured functionally on a second level of the functional hierarchy as one or more processors (5) or parts of one or more processors (5), at least one processor constituting a central processing unit or microprocessor (5) in the data processing device, and possible further processors optionally being configured as control and/or communication processors respectively.

20. A scaleable integrated data processing device according to claim 19, wherein the central processing unit

(5) is configured functionally on a third level of the functional hierarchy as a parallel processor with several execution units working in parallel provided in one and the same layer (P, MP) or in two or more layers (P, MP) or in sublayers thereof to provide an optimal interconnection topology.

Cont. B1

21. A scaleable integrated data processing device according to claim 19, wherein more than one central processing unit is provided, wherein each central processing unit (5) is mutually interconnected and adapted for working in parallel and provided in one and the same layer (P, MP) or in two or more layers (P, MP) to provide an optimal interconnection topology.

22. A scaleable integrated data processing device according to claim 19, wherein the storage unit in a layer (M,MP) is configured functionally on the second level of the functional hierarchy as one or more memories or parts of one or more memories, at least one memory constituting a RAM and being connected with at least one control processing unit or microprocessor, and possible further memories optionally being configured as high-speed memories, ROMs, WORM, ERASABLE and REWRITEABLE respectively.

23. A scaleable integrated data processing device according to claim 22, wherein two or more RAMs (6) are connected to a central processing unit (5) and respectively assigned to two or more subunits in the central processing unit (5), RAMs (6) and the subunits being distributed in selected combinations in one or more layers (P, M, MP) to provide an optimal interconnection topology.

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24. A scaleable integrated data processing device according to claim 22, wherein two or more central processing units (5) are provided which are connected with one or more common RAM or RAMs (6), and each central processing unit is provided in mutually adjacent layers (P, MP), or distributed in selected combinations between two or more layers (P, MP), and that the common RAM or RAMs are provided in selected combinations in one or more of the layers (P, MP) and/or in one or more memory layers (M) adjacent to the latter or interfoliated there between to provide an optimal interconnection topology.

25. A scaleable integrated data processing device according to claim 22, wherein at least a part of the storage unit constitutes a mass memory, the mass memory optionally being configured as RAM, ROM, WORM, ERASABLE or REWRITEABLE or combinations thereof.

26. A scaleable integrated data processing device according to claim 18, wherein the data processing unit comprises several processor layers (P) and several memory layers (M), and the memory layers (M), in order to reduce the signal paths there between and the processor layers (P), are interfoliated between the latter.

Cont. B1

27. A scaleable integrated data processing device according to claim 17, wherein further electrical structures are provided as electrical edge connections on or over at least one side edge of one or more layers (P,M,MP) in order to contact electrical conducting structures in other layers and/or provide electrical connection between layers and substrate.

28. A scaleable integrated data processing device according to claim 17, wherein the further electrical conducting structures are provided as vertical conducting structures in one or more layers (P, M, MP) and form electrical connections in the cross-direction of the layers and perpendicular to their planes in order to contact electrical conducting structures in other layers and/or to provide electrical connection between the layers and substrate.

29. A scaleable integrated data processing device according to claim 17, wherein one or more layers (P, M, MP) are formed of an organic thin-film material, the organic thin-film material or materials selected from the group consisting of monomeric, oligomeric and polymeric organic materials and metal-organic complexes, and combinations thereof.

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30. A scaleable integrated data processing device according to claim 29, wherein all layers (P, M, MP) are formed of organic thin-film material.

31. A scaleable integrated data processing device according to claim 17, wherein one or more layers (P, M, MP) are formed of inorganic thin-film material, the inorganic thin-film material or materials being selected from the group consisting of crystalline, polycrystalline and amorphous thin-film materials, and combinations thereof.

32. A scaleable integrated data processing device according to claim 17, wherein two or more layers (P, M, MP) are formed of both organic and inorganic thin-film materials or combinations thereof, the organic thin-film material or materials being selected from the group consisting of monomeric, oligomeric and polymeric organic materials and metal-organic complexes, and combinations thereof, and the